**TITLE OF INVENTION**: LOW VOLTAGE ELECTRON SOURCE WITH SELF ALIGNED GATE APERTURES, FABRICATION METHOD THEREOF, AND LUMINOUS DISPLAY USING THE ELECTRON SOURCE

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Version with Marking to Show Changes Made and Related Remarks /Arguments

**1. Specification:**

a. Paragraph [0033]

The electron source as is described above become addressable when: the first cathode electrode is configured as multiple cathode electrodes each electrically isolated from each other; ~~the nano-structures in the emitter layer are distributed as multiple patches along the cathode electrodes;~~ the gate electrode is configured as multiple gate electrodes, each electrically isolated from each other and intersects with the multiple cathode electrodes ~~at the patches of nano-structures~~; and apertures are formed at the intersection in the gate electrode and the insulator, each exposes and is aligned with one nano-structure from the emitter layer. Activation of a selected cathode and a selected gate electrode will determine one intersection that emits electrons.

REMARKS:

FIG. 3C. The catalyst, Ni for example, can be deposited by thermal or e-beam evaporation, or electrochemical plating through an ion-track-etched membrane laid on top of the substrate.

REMARKS:

*3 nm is more accurate than 10 nm, although 10 nm is acceptable also.*

*Evaporation and electrochemical plating are the two most common ways to deposit catalyst.*

d. Paragraph [0076]

Optionally, eEither the diffusion barrier or the ballast resistor layer can be deposited at the same time when the catalyst is deposited through the track-etched membrane.

REMARKS;

*Neither diffusion barrier nor ballast resistor layer has to be deposited at the same time when the catalyst is deposited.*

e. Insertion between paragraph [0078] and [0079]:

In both the embodiments shown in FIG.8 and FIG. 9, the nano-structures are distributed along and over the cathode electrodes in patches. However, this is not necessary for an electron source or display to be addressable. In fact, the nano-structures can be distributed continuously either over and along the cathodes or over the entire substrate. Since only at the intersections where both cathode and gate electrodes are present, the nano-structures at other locations will not emit electrons. It should also be pointed out that when a conductive material is used to embed the nano-structures in an addressable electron source or display, care must be taken to maintain the electrical isolation between the cathodes. Using a non-conductive material to fill the space between the cathodes should solve the problem.

*The nano-structures do not have to be distributed in patches along the cathode in order for the electron source to be addressable. See the added paragraph between [0078] and [0079] for explanation.*

b. Paragraph [0036]

The display device described above become fully addressable, when: the cathode electrode is configured as array of strip-like cathode electrodes extending substantially in the same direction and to be spaced and electrically insulated from each other at intervals in the transverse direction; ~~the nano-structures in the emitter layer are distributed as patches along the cathode electrodes;~~ the gate electrode is configured as array of strip-like gate electrodes extending in the direction that intersect with the cathode electrodes ~~at the patches of nano-structures~~ and to be spaced and electrically insulated from each other at intervals in the transverse direction; one or an array of apertures are formed in the gate electrode and the gate insulator at intersections, each aligned with and exposes one nano-structure in the emitter layer; and the anode electrode is configured as an array of strip-like anode electrodes, each extending opposed to a corresponding gate electrodes. The intersection forms a pixel region corresponding to one pixel of a display.

REMARKS:

*The nano-structures do not have to be distributed in patches along the cathode in order for the display to be addressable. See the added paragraph between [0078] and [0079] for explanation.*

c. Paragraph [0068]

FIG. 3 depicts one of the possible fabrication process flows for the source shown in FIG. 2. Starting with an insulating substrate 40, such as a Si wafer or a glass plate, shown in FIG. 3A, a cathode metal 30, Cr for example, is deposited on to the substrate, as is shown in FIG. 3B. A patterned catalyst layer 50 of 3~~1~~0 nm thick~~ness~~ is then deposited onto the cathode, as is shown in